

PHB/PHD/PHU108NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 03 — 18 April 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Lead-free construction
- Very low on-state resistance
- Low gate charge

1.3 Applications

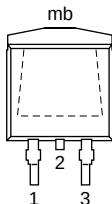
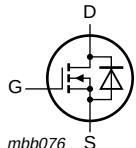
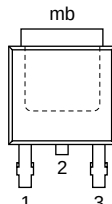
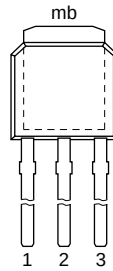
- DC-to-DC converter
- Switch-mode power supplies

1.4 Quick reference data

- $V_{DS} \leq 25 \text{ V}$
- $R_{DS(on)} \leq 6 \text{ m}\Omega$
- $I_D \leq 75 \text{ A}$
- $Q_{gd} = 5.6 \text{ nC (typ)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D) ^[1]		
3	source (S)		
mb	mounting base; connected to drain		
			
		SOT404 (D2PAK)	
		SOT428 (DPAK)	
		SOT533 (IPAK)	

[1] It is not possible to make a connection to pin 2 of the SOT404 and SOT428 packages.

PHILIPS

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PHB108NQ03LT	D2PAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT404
PHD108NQ03LT	DPAK	plastic single-ended surface mounted package; 3 leads (one lead cropped)	SOT428
PHU108NQ03LT	IPAK	plastic single-ended package; 3 leads (in-line)	SOT533

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

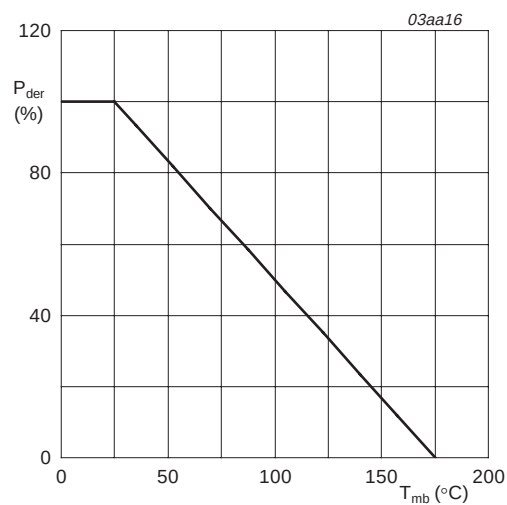
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2 and 3	-	75	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	187	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A

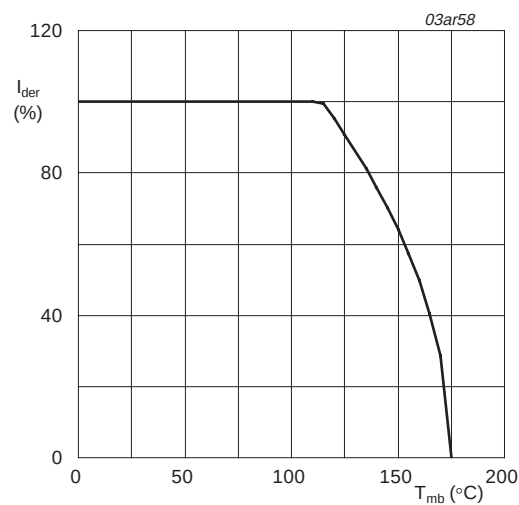
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}$; $t_p = 0.25\text{ ms}$; $V_{DD} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	180	mJ
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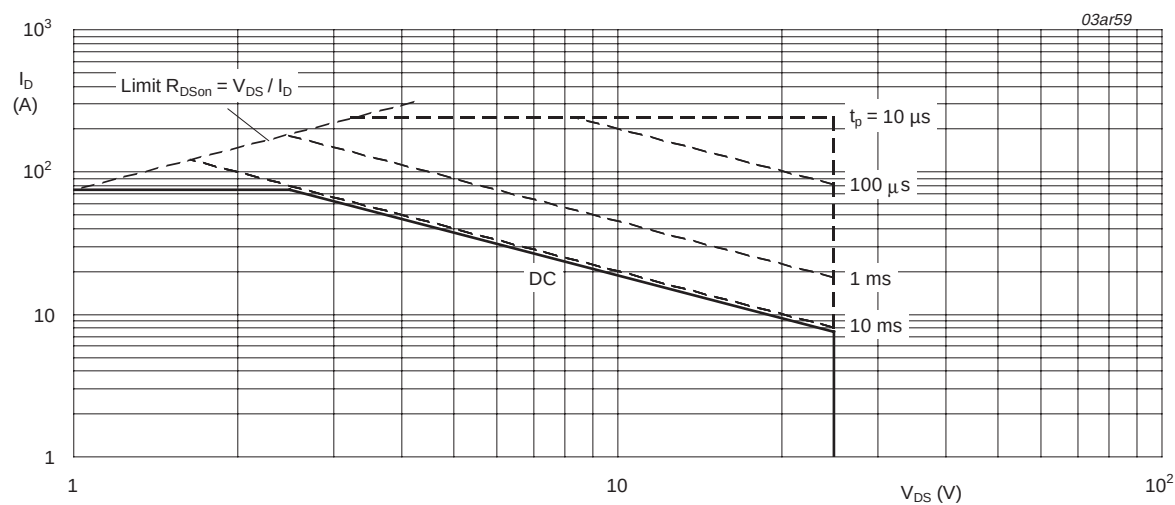
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 5V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT404	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
	SOT428	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	75	-	K/W
		mounted on a printed-circuit board; vertical in still air; SOT404 minimum footprint	-	50	-	K/W
	SOT533	vertical in free air	-	70	-	K/W

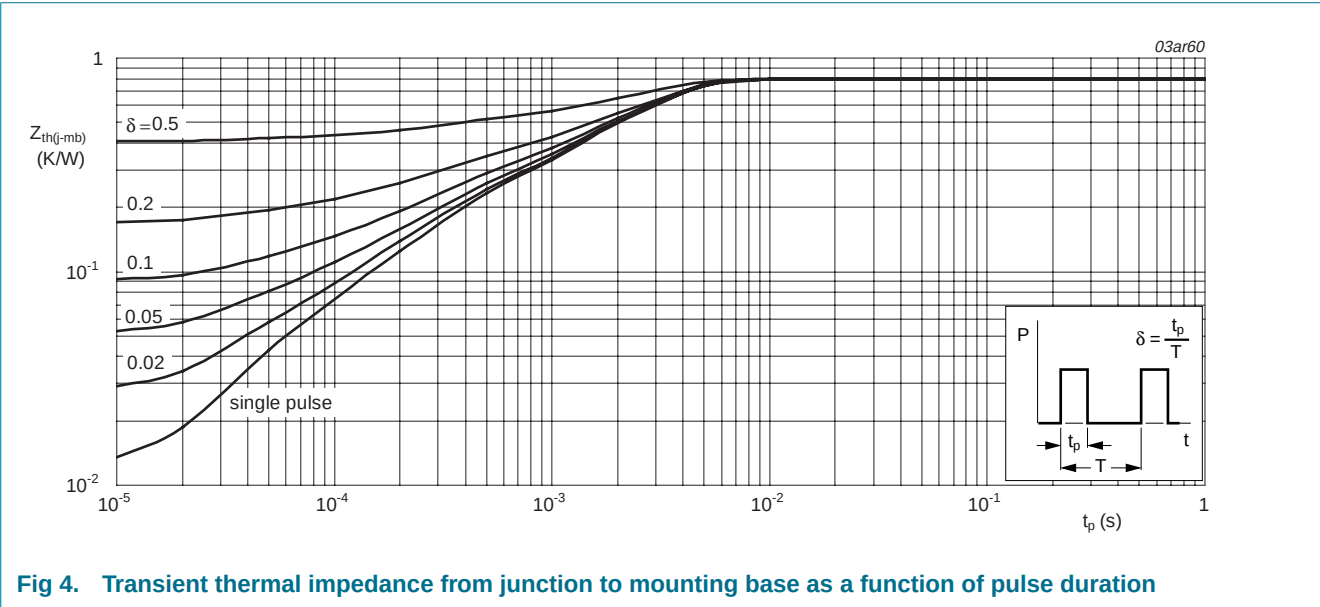
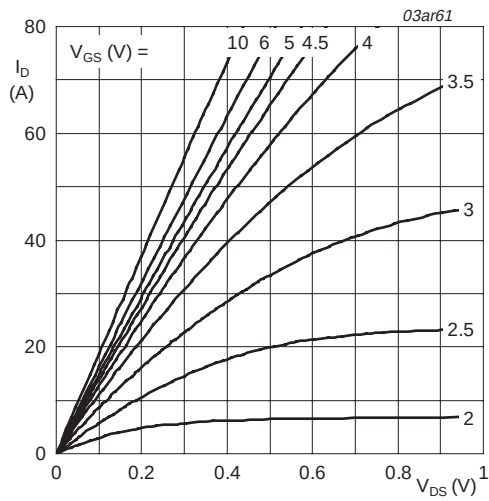


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

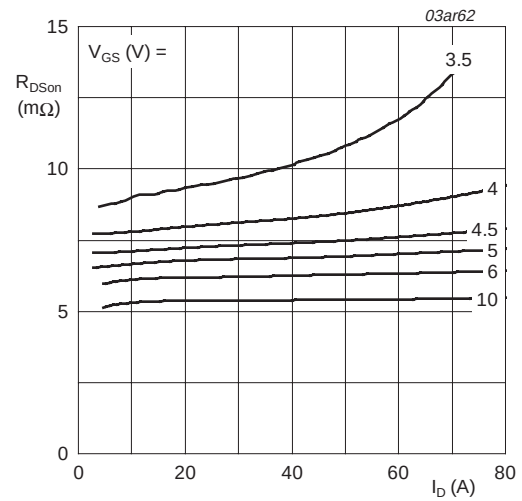
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	25	-	-	V
		$T_j = -55\text{ °C}$	22	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.2	V
I_{DSS}	drain-source leakage current	$V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	-	1	μA
		$T_j = 175\text{ °C}$	-	-	500	μA
R_G	gate resistance	$f = 1\text{ MHz}$	-	1.2	-	Ω
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	0.02	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; Figure 6 and 8				
		$T_j = 25\text{ °C}$	-	6.7	7.5	m Ω
		$T_j = 175\text{ °C}$	-	12.1	13.5	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; Figure 6 and 8	-	5.3	6	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; $V_{GS} = 4.5\text{ V}$; Figure 11 and 12	-	16.3	-	nC
Q_{gs}	gate-source charge		-	4	-	nC
Q_{gs1}	pre- $V_{GS(th)}$ gate-source charge		-	2.5	-	nC
Q_{gs2}	post- $V_{GS(th)}$ gate-source charge		-	1.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	5.6	-	nC
V_{plat}	plateau voltage		-	2.4	-	V
$Q_{g(tot)}$	total gate charge	$I_D = 0\text{ A}$; $V_{DS} = 0\text{ V}$; $V_{GS} = 4.5\text{ V}$	-	12.5	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $f = 1\text{ MHz}$; Figure 14	-	1375	-	pF
C_{oss}	output capacitance		-	640	-	pF
C_{rss}	reverse transfer capacitance		-	250	-	pF
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ V}$; $f = 1\text{ MHz}$	-	2120	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}$; $R_L = 0.5\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 5.6\text{ }\Omega$	-	15	-	ns
t_r	rise time		-	38	-	ns
$t_{d(off)}$	turn-off delay time		-	32	-	ns
t_f	fall time		-	25	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 13	-	0.86	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_R = 25\text{ V}$	-	34	-	ns
Q_r	recovered charge		-	21	-	nC



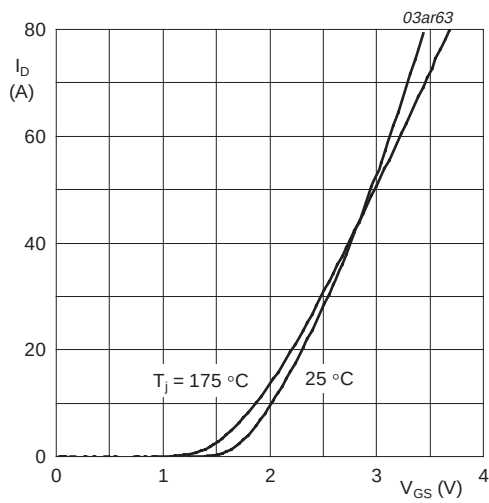
$T_J = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



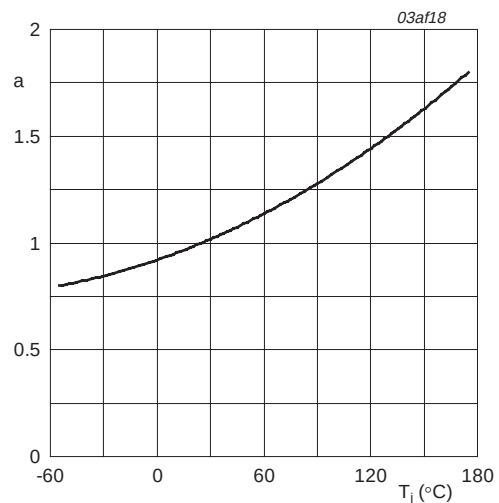
$T_J = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



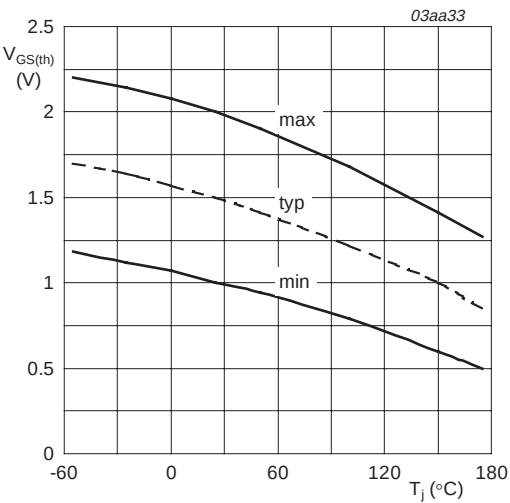
$T_J = 25^\circ\text{C}$ and 175°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



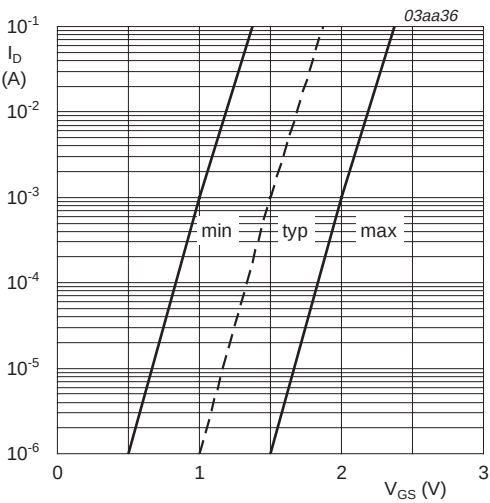
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



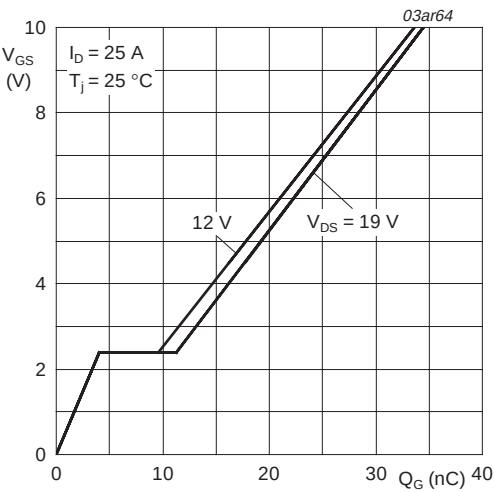
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^{\circ}\text{C}; V_{DS} = 5\text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25\text{ A}; V_{DS} = 12\text{ V and } 19\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

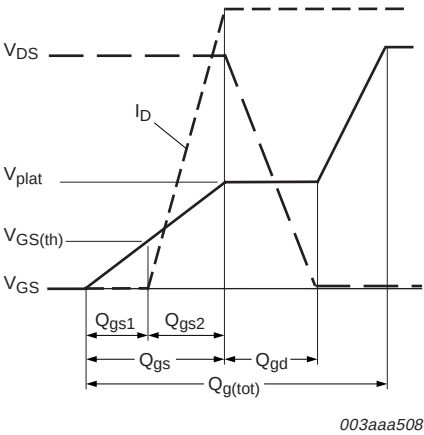
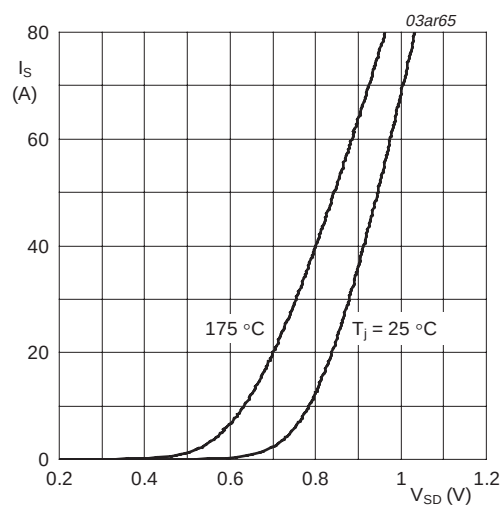
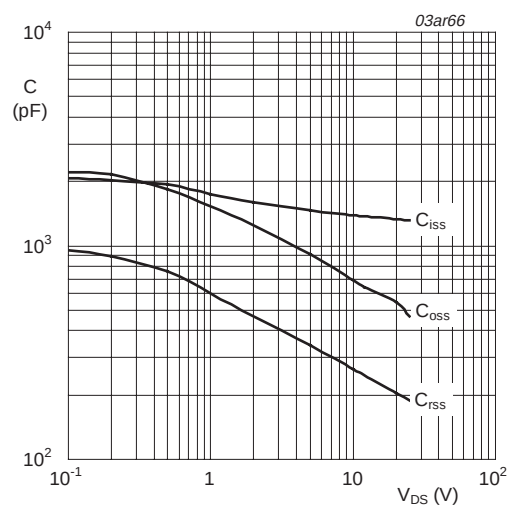


Fig 12. Gate charge waveform definitions



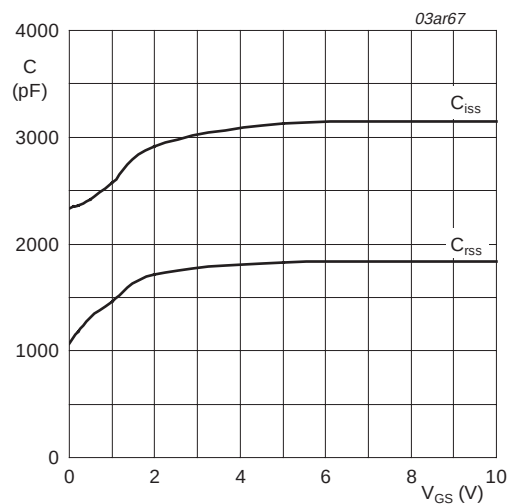
$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}$

Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

7. Package outline

Plastic single-ended surface mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

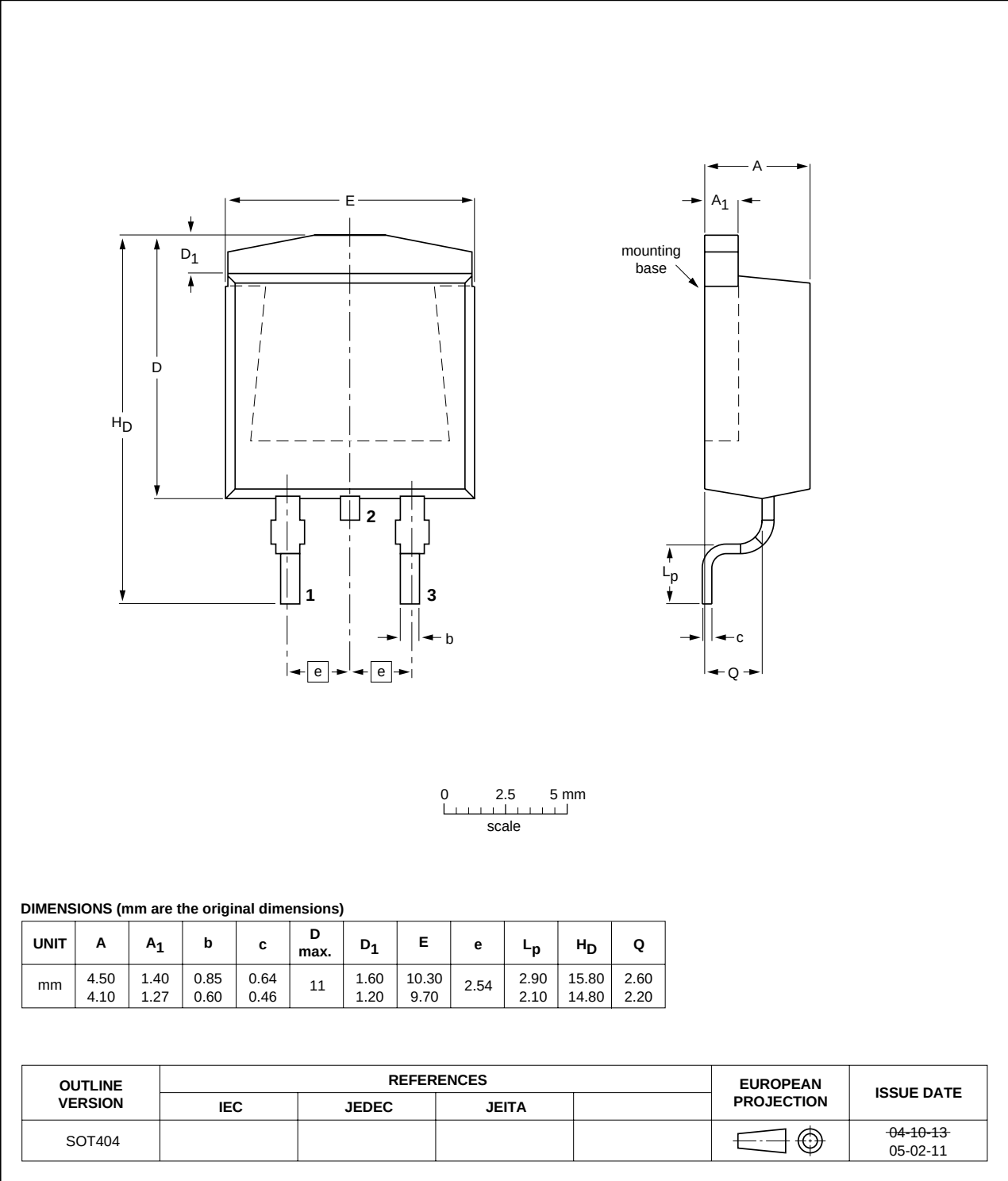
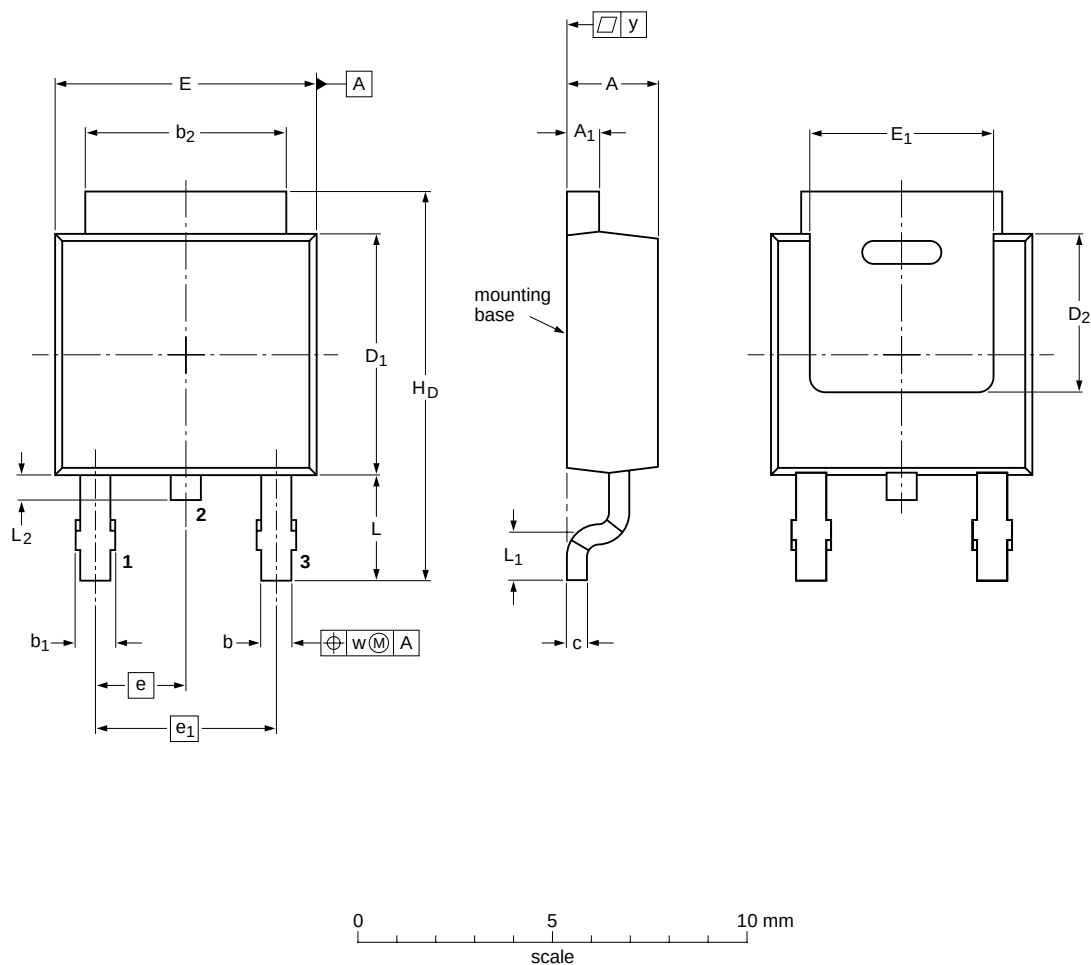


Fig 16. Package outline SOT404 (D2PAK)

Plastic single-ended surface mounted package (DPAK); 3 leads (one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

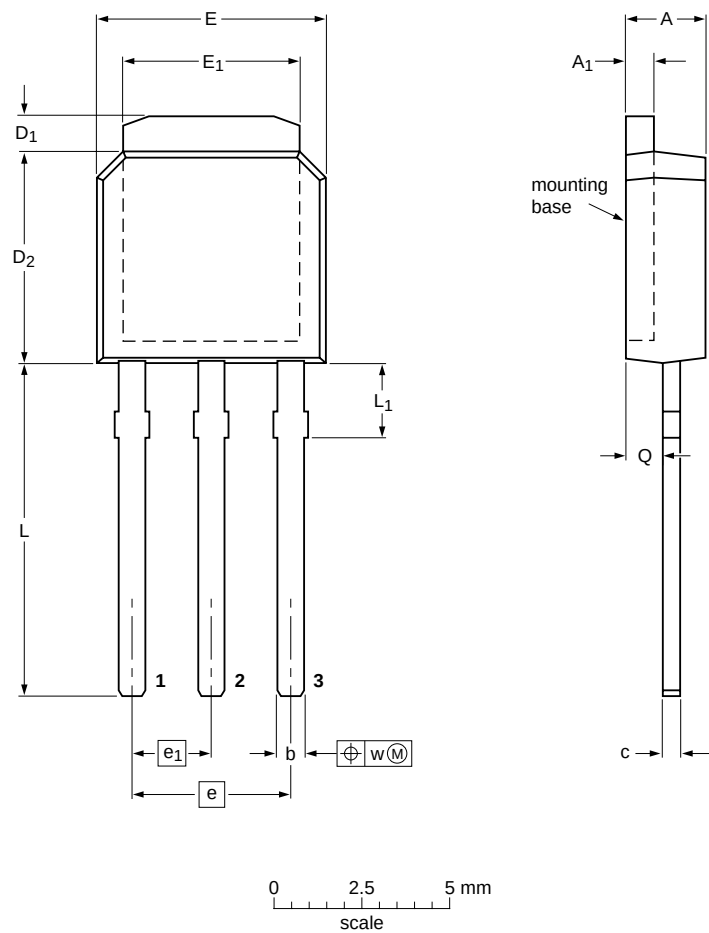
UNIT	A	A ₁	b	b ₁	b ₂	c	D ₁	D ₂ min	E	E ₁ min	e	e ₁	H _D	L	L ₁ min	L ₂	w	y max
mm	2.38 2.22	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			05-02-09 05-02-11

Fig 17. Package outline SOT428 (DPAK)

Plastic single-ended package (IPAK); 3 leads (in-line)

SOT533



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D ₁	D ₂	E	E ₁	e	e ₁	L	L ₁ ⁽²⁾ max	Q	w
mm	2.38 2.22	0.89 0.71	0.89 0.71	0.56 0.46	1.10 0.96	6.23 5.97	6.73 6.47	5.21 5.00	4.57 BSC ⁽¹⁾	2.285 BSC ⁽¹⁾	9.6 9.2	2.7	1.1 1.0	0.3

- Notes
1. Basic spacing between centers.
 2. Terminal dimensions are uncontrolled within zone L₁.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT533		TO-251				04-09-22 05-02-11

Fig 18. Package outline SOT533 (IPAK)



8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PHB_PHD_PHU108NQ03LT_3	20050418	Product data sheet	2004070095	9397 750 14707	PHP_PHB_PHD108NQ03LT-02
Modifications:					
• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Removal of PHP108NQ03LT • Addition of PHU108NQ03LT • Section 4 “Limiting values” I_D, I_{DM}, P_{tot} and I_{SM} data corrected. • Table 5 “Characteristics” $R_{DS(on)}$, $Q_{g(tot)}$, Q_{gs}, Q_{gd}, C_{iss}, C_{oss}, C_{rss}, $t_{d(on)}$, t_r, $t_{d(off)}$, t_f and Q_r test conditions and/or typical values modified. • Table 5 “Characteristics” R_G, Q_{gs1}, Q_{gs2} and V_{plat} tests added. • Table 5 “Characteristics” $V_{GS(th)}$, C_{iss}, C_{rss} and $Q_{g(tot)}$ data added. • Figure 2, 3, 4, 5, 6, 7, 8, 11, 13 and 14 modified. • Figure 12 and 15 added.					
PHP_PHB_PHD108NQ03LT-02	20020911	Product data	-	9397 750 10159	PHP_PHB_PHD108NQ03LT-01
PHP_PHB_PHD108NQ03LT-01	20011218	Product data	-	9397 750 09065	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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11. Disclaimers

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13. Contact information

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For sales office addresses, send an email to: sales.addresses@www.semiconductors.philips.com



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